BIJU PATNAIK UNIVERSITY OF TECHNOLOGY, ORISSA

Syllabus for M.Tech in VLSI & Embedded System Design

Semester	Subject	Credit	Details of Subjects
I	VLPC-101	4	HDL and High Level Synthesis
	VLPC-102	4	Digital Integrated Circuit Design
	VLPC-103	4	Semiconductor Device Modeling and Simulation
		3	**Electives – I** (***any one***)
	VLPE-101		VLSI Fabrication Technology
	VLPE-102		VLSI Digital Signal Processing Systems
	VLPE-103		VLSI Testing
		3	**Electives – II** (***any one***)
	VLPE-104		Analogue Integrated Circuit Design
	VLPE-105		VLSI Physical Design
	VLPE-106		Reliability and Testability of IC Design
	VLPR-101	4	EDA Lab
	VLPT-101	2	Seminar on Pre-thesis work-1
Semester Credits:		**24**	
II	PC-4	4	Embedded System Design
	PC-5	4	RF and Mixed-Signal Integrated Circuits
	EL-3	3	Microsystems – Principles, Design and Application
	(***any one***)		Analogue and Mixed-Signal Testing
			VLSI and MEMS Packaging
	EL-4	3	ASIC and SoC Design
	(***any one***)		Low Power Digital VLSI Design
			Emerging Topics in IC Design
	EL-5	3	Introduction to Nanoelectronics
	(***any one***)		Statistical Signal Processing
			Adaptive Signal Processing
	Lab-2	4	Embedded System Lab
	Seminar-2	2	Seminar on Pre-thesis work-2
	Viva-1	2	Comprehensive Viva-Voce - I
Semester Credits:		**25**	

Semester	Subject	Credit	Details of Subjects
III	**Open Elective (any one)**	**3**	Project Management / Project Costing / Technology Management / Research Methodology / Optimization Techniques / Computational Intelligence /
	Thesis-1	**14**	Thesis – I
Semester Credits:		**17**	
IV	Thesis -2	20	Thesis – II
	Seminar-2	2	Seminar
	Viva-2	2	Comprehensive Viva-Voce – II
Semester Credits:		**24**	
Total Credits		**90**	

HDL and High Level Synthesis (3 – 1 – 0) Credits: 4

MODULE – I **(13 hours)**

Structured Design Concepts:

The Abstraction Hierarchy, Textual vs. Pictorial Representations, Types of Behavioral Descriptions, Design Process, Structural Design Decomposition, The Digital Design Space

Design Tools:

CAD Tool Taxonomy, Schematic Editors, Simulators, The Simulation System, Simulation Aids, Applications of Simulation, Synthesis Tools

Basic Features of VHDL:

Major Language Constructs, Lexical Description, VHDL Source File, Data Types, Data Objects, Language Statements, Advanced Features of VHDL, The Formal Nature of VHDL, VHDL 93

Basic VHDL Modeling Techniques:

Modeling Delay in VHDL, The VHDL Scheduling Algorithm, Modeling Combinational and Sequential Logic, Logic Primitives

MODULE – II **(13 hours)**

Algorithmic Level Design:

General Algorithmic Model Development in the Behavioral Domain, Representation of System Interconnections, Algorithmic Modeling of Systems

Register Level Design:

Transition from Algorithmic to Data Flow Descriptions, Timing Analysis, Control Unit Design, Ultimate RISC Machine

Gate Level; and ASIC Library Modeling:

Accurate Gate Level Modeling, Error Checking, Multivalued Logic for Gate Level Modeling, Configuration Declarations for Gate Level Models, Modeling Races and Hazards, Approaches to Delay Control

HDL-Based Design Techniques:

Design of Combinational Logic Circuits, Design of Sequential Logic Circuits

MODULE – III **(14 hours)**

ASICs and the ASIC Design Process:

What is an ASIC?, ASIC Circuit Technology, Types of ASICs, The ASIC Design Process, FPGA Synthesis

Modeling for Synthesis:

Behavioral Model Development, The Semantics of Simulation and Synthesis, Modeling Sequential Behavior, Modeling Combinational Circuits for Synthesis, Inferred Latches and Don't Cares, Tristate Circuits, Shared Resources, Flattening and Structuring, Effect of Modeling Style on Circuit Complexity

Integration of VHDL into a Top-Down Design Methodology:

Top-Down Design Methodology, Sobel Edge Detection Algorithm, System Requirements Level, System Definition Level, Architecture Design, Detailed Design at the RTL Level, Detailed Design at the Gate Level

Synthesis Algorithms for Design Automation:

Benefits of Algorithmic Synthesis, Algorithmic Synthesis Tasks, Scheduling Techniques, Allocation Techniques, State of the Art in High-Level Synthesis, Automated Synthesis of VHDL Constructs

Textbooks:

1. James R. Armstrong and F. Gail Gray, ***VHDL Design Representation and Synthesis***, Prentice Hall, 2000.

Recommended Reading:

1. A.M. Dewey, ***Analysis and Design of Digital Systems with VHDL***, PWS Kent, 1996.
2. A.A. Jerraya, H. Ding and P. Kission, ***Behavioral Synthesis and Component Reuse with VHDL***, Kluwer, 1996.
3. K.C. Chang, ***Digital System Design with VHDL and Synthesis: An Integrated Approach***, Wiley India Pvt. Ltd., New Delhi

Digital Integrated Circuit Design

(3 – 1 – 0) Credits: 4

MODULE – I **(13 hours)**

Introduction, Design Metrics and Manufacturing Process:

A Historical Perspective, Issues in Digital Integrated Circuit Design, Quality Metrics of a Digital Design, Introduction to Manufacturing Process, Manufacturing CMOS Integrated Circuits, Design Rules – The Contract between Designer and Process Engineer, Packaging Integrated Circuits

The Devices:

Introduction, The Diode, The MOS(FET) Transistor, The Wire, Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, SPICE Wire Models

The CMOS Inverters and CMOS Logic Gates – the Static View:

Introduction to CMOS Inverter, The Static CMOS Inverter – An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter, Introduction to Static CMOS Design, Complementary CMOS, Ratioed Logic, Pass-Transistor Logic

CMOS Inverter – the Dynamic View:

Performance of CMOS Inverter: The Dynamic Behavior, Power, Energy, and Energy-Delay, Perspective: Technology Scaling and its Impact on the Inverter Metrics

MODULE – II **(13 hours)**

Dynamic CMOS Logic, Timing Metrics:

Dynamic CMOS Design, CMOS Logic Design Perspectives, Timing Metrics: Timing Metrics for Sequential Circuits, Classification of Memory Elements

Static and Dynamic Sequential Circuits:

Static Latches and Registers, Dynamic Latches and Registers, Alternative Register Styles: Pulse Registers and Sense-Amplifier Based Registers, Pipelining: An Approach to Optimize Sequential Circuits – Latch Vs Register-Based Pipelines and NORA-CMOS – A Logic Style for Pipelined Structures, Nonbistable Sequential Circuits

Coping with Interconnect:

Introduction, Capacitive Parasitics, Resistive Parasitics, Inductive Parasitics, Advanced Interconnect Techniques, Networks-on-a-Chip

Timing Issues in Digital Circuits:

Introduction, Timing Classification of Digital Systems, Synchronous Design – An In-depth Perspective, Self-Timed Circuit Design, Synchronisers and Arbiters, Clock Synthesis and Synchronisation Using a Phase-Locked Loop, Future Directions and Perspectives

MODULE – III **(14 hours)**

Designing Arithmetic Building Blocks:

Introduction, Datapaths in Digital Processor Architecture, The Adder, The Multiplier, The Shifter, Other Arithmetic Operators, Power and Speed Trade-off's in Datapath Structures, Perspective: Design as a Trade-off

Designing Memory and Array Structures:

Introduction, The Memory Core, Memory Peripheral Circuitry, Memory Reliability and Yield, Power Dissipation in Memories, Case Studies in Memory Design: The PLA, A 4-Mbit SRAM and A 1-Gbit NAND Flash memory, Perspective: Semiconductor Memory Trends and Evolution

Validation and Test of Manufactured Circuits:

Introduction, Test Procedure, Design for Testability, Test Pattern Generation

Textbooks:

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, ***Digital Integrated Circuits – A Design Perspective*****,** 2nd edn., Pearson Education, 2003. ISBN: 8178089912.

Recommended Reading:

1. K. Eshraghian, and N.H.E. Weste, ***Principles of CMOS VLSI Design – a Systems Perspective***, 2nd edn., Addison Wesley, 1993.
2. Wayne Wolf, ***Modern VLSI Design System – on – Chip Design***, 3rd edn., Pearson Education, 2003.
3. M. Michael Vai, ***VLSI Design***, CRC Press, 2001.
4. John P. Uyemura, ***CMOS Logic Circuit Design***, Springer (Kluwer Academic Publishers), 2001.
5. Ken Martin, ***Digital Integrated Circuit Design***, Oxford University Press, 2000.

Semiconductor Device Modeling and Simulation (3–1–0) Credits: 4

MODULE – I (13 hours)

Semiconductor Electronics Review:
Elements of Semiconductor Physics, Physical Operation of a ***PN*** Junction, MOS Junction, MS Junction

PN–Junction Diode and Schottky Diode:
DC Current-Voltage Characteristics, Static Model, Large-Signal Model, Small-Signal Model, Schottky Diode and its Implementation in SPICE2, Temperature and Area Effects on the Diode Model Parameters, SPICE3, HSPICE and PSPICE Models

Bipolar Junction Transistor (BJT):
Transistor Convention and Symbols, Ebers-Moll Static Model, Ebers-Moll Large-Signal Model, Ebers-Moll Small-Signal Model, Gummel-Poon Static Model, Gummel-Poon Large-Signal Model, Gummel-Poon Small-Signal Model, Temperature and Area Effects on the BJT Model Parameters, Power BJT Model, SPICE3, HSPICE and PSPICE Models

MODULE – II (13 hours)

Junction Field-Effect Transistor (JFET):
Static Model, Large-Signal Model and its Implementation in SPICE2, Small-Signal Model and its Implementation in SPICE2, Temperature and Area Effects on the JFET Model Parameters, SPICE3, HSPICE and PSPICE Models

Metal-Oxide-Semiconductor Transistor (MOST):
Structure and Operating Regions of the MOST, LEVEL1 Static Model, LEVEL2 Static Model, LEVEL1 and LEVEL2 Large-Signal Model, LEVEL3 Static Model, LEVEL3 Large-Signal Model, The Effect of Series Resistances, Small-Signal Models, The Effect of Temperature, BSIM1, BSIM2, SPICE3, HSPICE and PSPICE Models

MODULE – III (14 hours)

BJT Parameter Measurements:
Input and Model Parameters, Parameter Measurements

MOST Parameter Measurements:
LEVEL1 Model Parameters, LEVEL2 Model (Long-Channel) Parameters, LEVEL2 Model (Short-Channel) Parameters, LEVEL3 Model Parameters, Measurements of Capacitance, BSIM Model Parameter Extraction

Noise and Distortions:

Noise, Distortion

Metal-Semiconductor Field-Effect Transistor (MESFET), Ion-Sensitive Field-Effect Transistor (ISFET) and Semiconductor-Controlled Rectifier (Thyristor):

The MESFET, The ISFET, The Thyristor

Textbooks:

1. Paolo Antognetti and Giuseppe Massobrio, ***Semiconductor Device Modeling with SPICE,*** 2nd edn., McGraw-Hill, New York, 1993, ISBN 0071349553 (paperback) or 007 0024693 (hardback).

Recommended Reading:

1. Richard S. Muller, Theodore I. Kamins, and Mansun Chan, ***Device Electronics for Integrated Circuits***, 3rd edn., John Wiley and Sons, New York, 2003. ISBN: 0-471-59398-2. Listed as D
2. H. Craig Casey, ***Devices for Integrated Circuits: Silicon and III-V Compound Semiconductors***, John Wiley, New York, 1999. Listed as DI
3. Dieter K. Schroder, ***Semiconductor Material and Device Characterization***, John Wiley and Sons, New York, 1990. Listed as S

VLSI Fabrication Technology

(3 – 0 – 0) Credits: 3

MODULE – I **(11 hours)**

Introduction:

Moore's Law and material processing, Defects in crystals, Eutectic phase diagram, Solid solubility, Homogeneous nucleation, Heterogeneous Nucleation, Growth processes

Crystal Growth:

Necking and dislocation free CZ crystal growth, Segregation of impurities along length and diameter, Defects in CZ crystals, FZ Crystal growth

Epitaxy:

Vapour phase epitaxy, LPE, MBE, CVD deposition of Polysilicon, SILOX Process

Diffusion:

Constant & limited source diffusion, Concentration dependent diffusion, Field assisted diffusion, Junction depth, Open tube and closed tube diffusion, Diffusion sources.

MODULE – II **(11 hours)**

Ion Implantation:

Basic process, Ion Implantation Systems, Ion penetration and profile, Ion Implantation Damage, Annealing

Oxidation:

Purpose, Dry and wet oxidation, Deal-Grove model, Oxidation system, Properties of oxides – Masking and charges in oxides

Deposition Processes:

Fundamentals of vacuum systems, Vacuum evaporation of thin films, DC and RF Sputtering of thin films, Interconnects, Contacts and dielectrics in IC Fabrication, Deposition of Silicon Nitride, Silicides and insulating layers

Lithography:

Pattern generation and mask making, Optical Lithography – Contact, Proximity and Projection Printing, Photoresists – Negative, Positive, Lift-off process, Electron beam and X-ray lithographic techniques.

MODULE – III **(12 hours)**

Etching:

Wet Etching, Isotropic and Anisotropic Etching, Plasma Etching, Reactive Ion Beam Etching.

IC Process Integration:

Bipolar Transistor Fabrication, Isolation techniques, P-MOS, N-MOS and C-MOS processes, IC Fabrication Process Integration, IC Process Yield and Reliability

MEMS Fabrication Processes:

Micro machining, Bulk Micro machining, Surface Micro machining, Deep RIE, Advanced Lithography, HEXIL & SCREAM Process, Polymer molding and LIGA Process

Text Books:

1. S.K. Gandhi, ***VLSI Fabrication Principles: Silicon and Gallium Arsenide***, Wiley India Pvt. Ltd., New Delhi, 2nd edn. (1994), ISBN: 0471580058.
2. Marc J. Madou, ***Fundamentals of Microfabrication***, CRC Press (2002), ISBN: 0849308267

Reference Books:

1. J. Plummer, M. Deal and P. Griffin, ***Silicon VLSI Technology***, Prentice Hall, 2000, ISBN: 0130850373.
2. S.M.Sze, ***VLSI Technology***, Tata McGraw Hill, 1983, ISBN: 0070582912.
3. S.Mahajan, ***Principles of Growth and Processing of Semiconductors***, McGraw Hill International Book Company, 1999, ISBN: 0070396051.
4. S.A.Campbell, ***The Science and Engineering of Microelectronics Fabrication***, Oxford University Press, ISBN: 0195105087.

VLSI Digital Signal Processing Systems (3 – 0 – 0) Credits: 3

MODULE – I (11 hours)

Introduction to DSP System:

Typical DSP algorithms, DSP application demands and scaled CMOS technology, Representation of DSP algorithms.

Iteration Bound:

Data-flow graph representations, Loop bound and iterartion bound, Algorithms for computing iteration bound, Iteration bound of multirate data-flow graphs.

Pipelining and Parallel Processing:

Pipelining of FIR digital filters, Parallel processing, Pipelining and parallel processing for low power.

Retiming:

Definitions and properties, Solving systems of inequalities, Retiming techniques.

MODULE – II (11 hours)

Unfolding:

An algorithm for unfolding, Properties of unfolding, Critical path, unfolding and retiming, Applications of unfolding.

Folding:

Folding transformation, Register minimization techniques, Register minimization in folding architectures, Folding of multirate systems.

Systolic Architecture Design:

Systolic array design methodology, FIR systolic arrays, Selection of scheduling vector, Matrix-matrix multiplication and 2D systolic array design, Systolic design for space representations containing delays.

MODULE – III (12 hours)

Bit-Level Arithmetic Architecture:

Parallel multipliers, Interleaved floor-plan and bit-plane-based digital filters, Bit-serial multipliers, Bit-serial filter design and implementation, Canonic signed digit arithmetic, Distributed arithmetic.

Programmable Digital Signal Processors:

Evolution of programmable digital signal processors, Important features of DSP processors, DSP processors for mobile and wireless communications, Processors for multimedia signal processing.

Textbooks:

1. K. K. Parhi, ***VLSI Digital Signal Processing Systems*, *Design and Implementation***, Wiley India Pvt. Ltd., New Delhi, ISBN 10: – 8126510986, ISBN – 13: 9788126510986.

Recommended Reading:

1. K.P. Keshab, ***VLSI Digital Signal Processing Systems: Design and Implementation***, Jacaranda Wiley, 1999.
2. Richard J, Higgins, ***Digital Signal Processing in VLSI***, Prentice Hall, ISBN-10: 013212887X, ISBN-13: 9780132128872
3. M.A. Bayoumi, ***VLSI Design Methodology for DSP Architectures***, Kluwer, 1994.

VLSI Testing

(3 – 0 – 0) Credits: 3

Module I **13 hours**

Introduction, Test Process and ATE (2 classes), Test Economics (1 class), Yield Analysis and Product Quality (1 class), Fault Modeling (2 classes), Logic Simulation (1 class), Fault Simulation (1 class), Testability Measures (2 classes), Combinational ATPG (3 classes).

Module II **13 hours**

Sequential ATPG (3 classes), Memory Test (4 classes), Analog Circuit Test (4 classes), Delay Test (2 classes)

Module III **12 hours**

IDDQ Testing (1 class), Design for Testability (3 classes), Built-In Self-Test (3 classes), Boundary Scan (2 classes), Analog Test Bus (1 class), System Test and Core Test (2 classes)

Textbook:

1. Michael L. Bushnell and Vishwani D. Agrawal, ***Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits***, B.S.Publications**,** 2000, ISBN 10: **–** 0792379918, ISBN-13: – 9780792379911.

Reference Books:

1. L.-T. Wang, C.-W. Wu, and X. Wen, ***VLSI Test Principles and Architectures: Design for Testability (Systems on Silicon)***, Morgan Kaufmann, ISBN 10: **–** 0123705975.
2. Alfred L. Crouch, ***Design-for-Test for Digital IC's and Embedded Core Systems***, Prentice Hall, ISBN 10: **–** 0130848271.
3. Niraj Jha and Sandeep Gupta, ***Testing of Digital Systems***, Cambridge University Press, 2003, ISBN 10: **–** 0521773563.

Analogue Integrated Circuit Design

(3 – 0 – 0) Credits: 3

MODULE – I **(11 hours)**

Introduction:

The MOS Transistor, I-V Characteristics, Equivalent Circuits, Noise

Resistor, Capacitors and Switches:

Integrated Resistors, Integrated Capacitors, Analog Switches, Layout of Switches

Basic Building Blocks:

Inverter with Active Load, Cascode, Cascode with Cascode Load, Source Follower, Threshold Independent Level Shift, Improved Output Stages

MODULE – II **(11 hours)**

Current and Voltage Sources:

Current Mirrors, Current References, Voltage Biasing, Voltage References

CMOS Operational Amplifiers:

General Issues, Performance Characteristics, Basic Architecture, Two Stages Amplifier, Frequency Response and Compensation, Slew Rate

MODULE – III **(12 hours)**

Operational Amplifiers and OTAs

Design of Two Stage OTAs: Guidelines, Single Stage Schemes, Class AB Amplifiers, Fully Differential Op-Amps, Micro-Power OTAs, Noise Analysis, Layout

CMOS Comparators:

Performance Characteristics, General Design Issues, Offset Compensation, Latches

Textbooks:

3. Franco Maloberti, ***Analog Design for CMOS VLSI Systems***, Kluwer Academic Publishers, 2001. ISBN: 0-7923-7550-5.

Reference Books:

1. Behzad Razavi, ***Design of Analog CMOS Integrated Circuits***, McGraw-Hill, 2001. ISBN: 0-07-238032-2.
2. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, ***Analysis and Design of Analog Integrated Circuit***, John Wiley & Sons, Inc., 4th edn., 2000. ISBN: 0-471-32168-0.
3. Phillip E. Allen and Douglas R. Holberg, ***CMOS Analog Circuit Design***, Oxford University Press, 2nd edn., 2002. ISBN: 0-19-511644-5
4. Johan H. Huijsing, ***Operational Amplifiers – Theory and Design,*** Kluwer. ISBN: 0792372840

VLSI Physical Design

(3 – 0 – 0) Credits: 3

MODULE – I **(11 hours)**

VLSI Physical Design Automation:

VLSI Design Cycle, Physical Design Cycle, Design Styles, System Packaging Styles, Historical Perspectives, Existing Design Tools

Design and Fabrication of VLSI Devices:

Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules, Layout of Basic Devices

Fabrication Process and its Impact on Physical Design:

Scaling Methods, Status of Fabrication Process, Issues Related to the Fabrication Process, Future of Fabrication Process, Solutions for Interconnect Issues, Tools for Process Development

MODULE – II **(11 hours)**

Data Structure and Basic Algorithms:

Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithm for Physical Design

Partitioning:

Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithm, Simulated Annealing and Evolution, Other Partitioning Algorithms, Performance Driven Partitioning

Floor Planning and Pin assignment:

Floor Planning, Chip Planning, Pin Assignment, Integrated Approach

MODULE – III **(12 hours)**

Placement:

Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement

Over-the-Cell Routing and Via Minimisation, Clock and Power Routing:

Over-the-Cell Routing, Via Minimisation, Clock Routing, Power and Ground Routing

Physical Design Automation of FPGAs:

FPGA Technologies, Physical Design Cycle for FPGAs, Partitioning, Routing

Physical Design Automation of MCMs:

MCM Technologies, MCM Physical Design Cycle, Partitioning, Placement, Routing

Text Books:

1. Naved A. Sherwani, ***Algorithms for VLSI Physical Design Automation***, 3rd Edn., Springer (India) Pvt. Ltd., 2005, ISBN: 0792383931

Reference Books:

1. Gerez, ***Algorithms for VLSI Design Automation***, Wiley India Pvt. Ltd., New Delhi, ISBN 10: – 8126508211, ISBN 13: – 9788126508211.

Reliability and Testability of IC Design (3 – 0 – 0)

MODULE – I **(11 hours)**

Basic Concepts, Quality and Reliability Assurance of Complex Equipments and Systems:

Introduction, Basic Concepts, Basic Tasks and Rules for Quality and Reliability Assurance of Complex Equipments and Systems

Probability Theory, Stochastic Process and Mathematical Statistics for Reliability Analysis:

Concept of Probability, Random Variables and Random Vectors, Distribution Functions used in Reliability Analysis, Limit Theorems, Renewal Processes, Regenerative and Semi-Regenerative Processes, Markov and Semi-Markov Processes, Non-regenerative Stochastic processes, Empirical Methods in Mathematical Statistics, Parameter Estimation, Testing Statistical Hypotheses

Reliability Analysis During the Design and Development Phases:

Introduction, Predicted Reliability of Equipments and Systems with Simple Structure, Reliability of Systems with Complex Structure, Reliability Allocation, Mechanical Reliability, Drift Failure, Failure Mode Analyses, Reliability Aspects in Design Reviews

MODULE – II **(11 hours)**

Qualification Tests for Components and Assemblies:

Basic Selection Criteria for Electronic Components, Qualification Tests for Complex Electronic Components, Failure Modes, Failure Mechanisms, and Failure Analysis of Electronic Components, Qualification Tests for Electronic Assemblies

Maintainability Analysis:

Maintenance and Maintainability, Maintenance Concepts, Maintainability Aspects in Design reviews, Predicted Maintainability, Basic Models for Spare Part Provisioning, Cost Considerations

Design Guidelines for Reliability, Maintainability and Software Quality:

Design Guidelines for Reliability, Design Guidelines for Maintainability, Design Guidelines for Software Quality

MODULE – III **(12 hours)**

Reliability and Availability of Repairable Systems – II:

Introduction and General Assumptions, One-Item Structure, Systems with Redundancy, 1-out-of-2 Redundancy, ***k***-out-of-***n*** Redundancy, Simple Series-Parallel Structures, Approximate Expressions for Large Series-Parallel Structures, Systems with Complex Structures, Computer-Aided Reliability and Availability Computations

Statistical Quality Control and Reliability Tests:

Statistical Quality Control, Statistical Reliability Tests, Statistical Maintainability Tests, Accelerated Testing, Goodness-of-fit Tests, Statistical Analysis of General Reliability Data

Quality and Reliability Assurance During the Production Phase:

Basic Activities, Testing and Screening of Electronic Components, Test and Screening Strategies, Economic Aspects, Reliability Growth

Text Books:

1. Alessandro Birolini, ***Reliability Engineering Theory and Practice***, 4th Edn., Springer (India) Pvt. Ltd., 2006, ISBN: 8181284518

Reference Books:

1. P.K. Lala, ***Digital Circuit Testing and Testability***, Academic Press, 1997

2. M.T.C. Lee, ***High-Level Test Synthesis of Digital VLSI Circuits***, Artech, 1997
3. P. Mazumdar and K. Chakreborty, ***Testing & Testable Design of High Density Random Access Memories***, Kluwer, 1996

2nd Semester

Embedded System Design (3 – 1 – 0)

MODULE – I **(13 hours)**

Introduction to Embedded Computing: Terms and scope, Application areas, Growing importance of embedded systems.

Specifications: Requirements, Models of computation, State Charts: Modeling of hierarchy, Timers, Edge labels and StateCharts semantics, Evaluation and extensions, General language characteristics: Synchronous and asynchronous languages, Process concepts, Synchronization and communication, Specifying timing, Using non-standard I/O devices, SDL, Petri nets: Introduction, Condition/event nets, Place/transition nets, Predicate/transition nets, Evaluation, Message Sequence Charts, UML, Process networks: Task graphs, Asynchronous message passing, Synchronous message passing, Java, VHDL: Introduction, Entities and architectures, Multi-valued logic and IEEE 1164, VHDL processes and simulation semantics, System C, Verilog and System Verilog, Spec C, Additional languages, Levels of hardware modelling, Language comparison, Dependability requirements.

MODULE – II **(13 hours)**

Embedded System Hardware: Introduction, Input: Sensors, Sample-and-hold circuits, A/D-converters, Communication: Requirements, Electrical robustness, Guaranteeing real-time behaviour, Examples, Processing units: Application-Specific Circuits (ASICs), Processors, Reconfigurable Logic, Memories, Output: D/A-converters, Actuators.

Standard Software: Embedded Operating Systems, Middleware, and Scheduling: Prediction of execution times, Scheduling in real-time systems: Classification of scheduling algorithms, Aperiodic scheduling, Periodic scheduling, Resource access protocols, Embedded operating systems: General requirements, Real-time operating systems, Middleware: Real-time data bases, Access to remote objects

MODULE – III **(14 hours)**

Implementing Embedded Systems: Hardware/Software Co-design: Task level concurrency management, High-level optimizations: Floating-point to fixed-point conversion, Simple loop transformations, Loop tiling/blocking, Loop splitting, Array folding, Hardware/software partitioning: Introduction, COOL, Compilers for embedded systems: Introduction, Energy-aware compilation, Compilation for digital signal processors, Compilation for multimedia processors, Compilation for VLIW processors, Compilation for network processors Compiler generation, retargetable compilers and design space exploration, Voltage Scaling and Power Management: Dynamic Voltage Scaling, Dynamic power management (DPM), Actual design flows and tools: SpecC methodology, IMEC tool flow, The COSYMA design flow, Ptolemy II, he OCTOPUS design flow.

Validation: Introduction, Simulation, Rapid prototyping and emulation, Test: Scope, Design for testability and Self-test programs, Fault simulation, Fault injection, Risk- and dependability analysis, Formal verification.

Textbooks:

1. Peter Marwedel, ***Embedded System Design***, Springer, 2006 http://ls12-www.cs.uni-dortmund.de/~marwedel/kluwer-es-book/

Recommended Reading:

1. Wayne Wolf, ***Computers as Components***, Morgan Kaufmann, 2001 http://www.ee.princeton.edu/~wolf/embedded-book
2. G. De Micheli, Rolf Ernst and Wayne Wolf, eds, ***Readings in Hardware/Software Co-Design***, Morgan Kaufmann, ***Systems-on-Silicon Series Embedded***
3. Frank Vahid and Tony D. Givargis, ***System Design: A Unified Hardware/Software Introduction***, Addison Wesley, 2002.
4. Michael Barr, ***Programming Embedded Systems in C and C++***, O'Reilly, 1999.
5. David E. Simon, ***An Embedded Software Primer***, Addison Wesley, 1999.

6. Jack Ganssle, The Art of Designing Embedded Systems, Newnes, 2000.
7. K. Short, ***Embedded Microprocessor System Design***, Prentice Hall, 1998.
C. Baron, J. Geffroy and G. Motet, ***Embedded System Applications***, Kluwer, 1997.

RF and Mixed-Signal Integrated Circuits (3 – 1 – 0)

MODULE – I **(13 hours)**

Introduction: Overview of wireless principles, Characteristics of passive IC components – resistors, Capacitors, Inductors, Transformers, Interconnect at RF and high frequencies, Skin effect.

Bandwidth Estimation Techniques: Method of open-circuit time constants, Method of short-circuit time constants, Rise time, Delay and Bandwidth.

High-frequency Amplifier Design: Zeros as bandwidth enhancers, Shunt-series amplifier, Bandwidth enhancement with f_T doublers, Tuned amplifiers, Neutralization and unilateralization, Cascaded amplifiers, AM-PM conversion.

MODULE – II **(13 hours)**

Voltage Reference: Review of diode behavior, Diodes and Bipolar Transistors in CMOS technology, Supply-independent bias circuits, Bandgap voltage reference, Constant-g_m bias.

Noise: Thermal noise, Short noise, Flicker noise, Popcorn noise, Classical two-port noise theory, Examples of noise calculations.

Low-Noise Amplifier (LNA) Design: Derivation of intrinsic MOSFET two-port noise parameters, LNA topologies – Power match Vs. Noise match, Power-constrained noise optimization, Design Example, Linearity and large signal performance, Spurious-free dynamic range.

MODULE – III **(14 hours)**

Mixers: Mixer fundamentals, Non-linear systems as linear mixers, Multiplier-based mixers, Sub-sampling mixers, Diode-ring mixers.

RF Power Amplifiers: Classes of power amplifiers, RF power amplifier design example, Power amplifier characteristics and Design consideration.

Phase-Locked Loops (PLL): Introduction to PLL, Linearized PLL models, Some noise properties of PLLs, Phase detectors, Sequential phase detectors, Loop filters and charge pumps, PLL design examples.

Oscillators and Synthesizers: Problems with purely linear oscillators, Describing functions, Resonators, Tuned oscillators, Negative resistance oscillators, Frequency synthesis.

Textbooks:

1. Thomas H. Lee, ***The Design of CMOS Radio-Frequency Integrated Circuits,*** 2nd Edn., Cambridge University Press, 2004.

Recommended Reading:

1. E.N. Farag and M.I. Elmasry, ***Mixed Signal VLSI Wireless Design: Circuits & Systems***, Kluwer, 1999.

Microsystems–Principles, Design and Application

(3 – 0 – 0)

MODULE – I **(11 hours)**

Introduction: MEMS, MEMS Processing, Micromachining, Wafer Bonding, LIGA, MEMS Examples, Scaling Laws

MEMS Materials: MEMS Materials, Silicon, Crystal Defects, Mechanical Properties of Materials, Beams and structures, Piezoelectric Materials, Piezoresistive Materials

MEMS Sensor: Resistive and Capacitive methods, Strain gauges, Piezoresistivity, MEMS Capacitive Sensors, MEMS Position sensor, MEMS Pressure sensor

MODULE – II **(11 hours)**

MEMS Sensor (Continued): MEMS Accelerometer, MEMS Gyroscope, MEMS Gas Sensors, Cantilever Sensors

MEMS Actuator: Electrostatic MEMS actuators, Comb drives, MEMS RF resonator, Scratch drive, Inchworm motor, Piezoelectric MEMS actuators, Thermal MEMS actuators, Magnetic MEMS actuators

MODULE – III **(12 hours)**

Optical MEMS: MEMS Infrared sensor, Digital Mirror Displays, Grating Light Valve Displays, Micro-optical elements

Micro-fluidics, Chemical MEMS: Microfluidics – Fluid flow, Electro-osmotic flow, Electrophoresis, Micropumps, Microvalves, Fabrication Process for microfuidic chip, Lab-on-a-Chip, µ-TAS, Inkjet Printer Head

Bio MEMS: DNA Analysis, Micro-array Gene Chip, Micro-surgery, Drug delivery

Text Books:

1. Stephen D. Senturia, ***Microsystem Design***, Kluwer Academic/Springer, 2nd edn. (2005), ISBN: 0792372468
2. R.S. Muller and A.P. Pisano, ***Micro Actuators***, IEEE Press, 2000.
3. P. Rai-Choudhury, ***Recent Advances in MEMS/MOEMS Technologies***, SPIE Press, 2000.
4. S.M. Sze, ***Semiconductor Sensors***, Wiley-Interscience Publishers, 1994.

5. T. Fukuda, and W. Menz, (Eds), ***Micro Mechanical Systems: Principles and Technology, Handbook of Sensors and Actuators***, Vol. 6, Elsevier, 1998.

Analogue and Mixed-Signal Testing (3 – 0 – 0)

MODULE – I **(11 hours)**

Overview of Mixed-Signal Testing – Mixed-signal circuits, Test and diagnostic equipments, Mixed-signal testing challenges, The Test Specification Process – Device datasheets, Generation of test plan, Components of a test program, DC and Parametric Measurements – Continuity, Leakage currents, Power supply currents, DC references and regulators, Impedance measurements, DC offset measurements, DC gain measurements, DC power supply rejection ratio, DC common-mode rejection ratio, Comparator DC tests, Voltage search techniques, DC tests for digital circuits, Measurement Accuracy – Terminology, Calibration and checkers, Dealing with measurement errors, Basic data analysis, Tester Hardware – Mixed-signal tester overview, DC resources, Digital subsystem, AC source and measurement, Time measurement system, Computing hardware.

MODULE – II **(11 hours)**

Sampling Theory – Analog measurements using DSP, Sampling and reconstruction, Repetitive sample sets, Synchronisation of smpling systems, DSP-Based Testing – Advantages of DSP-based testing, Digital signal processing, Discrete-time transforms, The inverse FFT, Analog Channel Testing – Overview, Gain and level tests, Phase tests, Distortion tests, Signal rejection tests, Noise tests, Simulation of analog channel tests, Sampled Channel Testing – Overview, Sampling considerations, Encoding and decoding, Sampled channel tests, Focused Calibrations – Overview, DC calibrations, AC amplitude calibrations, Other Ac calibrations, Error cancellation techniques.

MODULE – III **(12 hours)**

DAC Testing – Basics of converter testing – intrinsic parameters versus transmission parameters, Comparison of DACs and ADCs, DAC failure mechanism, Basic DC tests, Transfer curve tests, Dynamic DAC tests, DAC architecture – Resistive divider DACs, Binary-weighted DACs, PWM DACs, Sigma-delta DACs, Companded DACs, Hybrid DAC architecture, Tests for common DAC applications – DC references, Audio reconstruction, Data modulation, Video signal generators, ADC Testing – ADC testing versus DAC testing, ADC code edge measurements – Edge code testing versus center code testing, Step search and binary search methods, Servo methods, Linear ramp histogram method, conversion from histograms to code edge transfer curves, Accuracy limitations of histogram testing, Rising ramps versus falling ramps, sinusoidal histogram method, DC tests and transfer curve tests, Dynamic ADC tests, ADC architecture – Successive approximation architecture, Intgrating ADCs (Dual slope and single slope), Flash ADCs, Semiflash ADCs, PDM (sigma-delta) ADCs, Test for common ADC applications – DC measurements, Audio digitization, Data transmission, Video digitization, DIB Design – DIB basics, Printed circuit boards, DIB traces, shields and guards, Transmission lines, Grounding and power distribution, BIB components, Common DIB circuits, Common DIB mistakes, Design for Test (DfT) – Overview of DfT and BIST, Advantages of DfT, Digital scan, Digital BIST, Digital DfT for mixed-signal circuits, Mixed-signal boundary scan and BIST, Adhoc mixed-signal DfT, Subtle forms of analog DfT, I_{DDQ} testing.

Text Books:

1. Mark Burns and Gordon W. Roberts, ***An Introduction to Mixed-Signal IC Test and Measurement***, Oxford University Press, 2001, ISBN: ISBN-10: 0195699262, ISBN-13: 9780195699265

Recommended Reading:

1. Bapiraju Vinnakota, ***Analog and Mixed-Signal Test***, Prentice Hall PTR, 1998, ISBN-10: 0137863101, ISBN-13: 978-0137863105
2. Prithviraj Kabisatpathy, Alok Barua, Satyabroto Sinha, ***Fault Diagnosis of Analog Integrated Circuits***, Springer, 2005, ISBN: 0-387-25742-X.
3. José Luis Huertas, Edited, ***Test and Design-for-Testability in Mixed-Signal Integrated Circuits***, Kluwer Academic Publishers, 2004, ISBN: 1-4020-7724-6.

VLSI and MEMS Packaging (3 – 0 – 0)

MODULE – I **(11 hours)**

Introduction: Basics of Electronic Packaging, Packaging Hierarchy in Electronic Systems, Functions of Packaging

Electric Considerations for Electronic Packaging: Electric Field Interference, Magnetic Field Interference, Noise performance due to passive components - Cabling, Shielding and Grounding/filtering/shielding/screening and surge protection/suppression, noise suppression

Thermal Considerations for Electronic Packaging: Heat generation and modes of heat transfer in electronic components and packages, Selection/Design of Heat Sinks, Ventilation, Forced cooling, Heat pipes for electronic cooling applications, Cooling of power intensive components

IC Packaging: Integrated Circuit Packages, Solder bumps, Direct Chip Attach, Multi-chip modules.

MODULE – II **(11 hours)**

IC Packaging (Continued): Microvia technology, LTCC

Testing and Reliability of Electronic Packages: Design for Test, Adhesive and Its Application, Thermal Management, Testing and Inspection, Package/Enclosure, Electronics Package Reliability and Failure Analysis, Product Safety and Third-Party Certification

PCB Fabrication and Design: PCB technology trends, multi-layer boards, Design CAD tool for PCB design, artwork and layout, general rules, design rules for PCB's for digital circuits, high frequency, analog and mixed signal circuits, power and microwave applications, Surface mount Technology

MODULE – III **(12 hours)**

Hybrid Electronic Packaging: Advantages of Hybrid packaging, Hybrid Fabrication Technology: Screen printing, conducting, resistive, dielectric and solder pastes, drying and firing, Hybrid assemblies

MEMS Packaging: MEMS Packaging Issues, Die Level Packaging, Wafer Level Packaging, Micro assembled caps, Sealing

Text Books:

1. Glenn R. Blackwell, ***The Electronic Packaging Handbook***, CRC Press, 2000, ISBN 0849385911
2. John H. Lau, ***Electronic Packaging: Design, Materials, Process, and Reliability***, McGraw-Hill, 1998, ISBN 0070371350

Recommended Reading:

1. Clyde F. Coombs, ***Printed Circuits Handbook***, McGraw-Hill, 2001, ISBN 0071350160
2. Rao R. Tummala, Eugene J. Rymaszewski, Alan G. Klopfenstein, (Eds), ***Microelectronics Packaging Handbook: Technology Drivers***, Vol. 1, Kluwer Academic Publishers, Second Edition, January 1997, ISBN: 0412084317

3. Rao R. Tummala, Eugene J. Rymaszewski, Alan G. Klopfenstein, (Eds), ***Microelectronics Packaging Handbook: Semiconductor Packaging***, Vol. 2, Kluwer Academic Publishers, Second Edition, January 1997, ISBN: 0412084414
4. Rao R. Tummala, Eugene J. Rymaszewski, Alan G. Klopfenstein, (Eds), ***Microelectronics Packaging Handbook: Technology***, Vol. 3, Kluwer Academic Publishers, Second Edition, January 1997, ISBN: 0412084511 PCB Design & Technology- Waller C. Bosshart, Tata McGraw-Hill

ASIC and SoC Design (3 – 0 – 0)

MODULE – I **(11 hours)**

Introduction: Voice over IP SOC, Intellectual Property, SOC Design Challenges, Design Methodology.

Overview of ASICs: Introduction, Methodology and Design Flow, FPGA to ASIC Conversion, Verification.

MODULE – II **(11 hours)**

SOC Design and Verification: Introduction, Design for Integration, SOC Verification, Set-Top-Box SOC, Set-Top-Box SOC Example. Summary. References.

Physical Design: Introduction, Overview of Physical Design Flow, Some Tips and Guidelines for Physical Design, Modern Physical Design Techniques.

MODULE – III **(12 hours)**

Low-Power Design: Introduction, Power Dissipation, Low-Power Design Techniques and Methodologies, Low-Power Design Tools, Tips and Guidelines for Low-Power Design.

Low-Power Design Tools: PowerTheater, PowerTheater Analyst, PowerTheater Designer.

Open Core Protocol (OCP): Highlights, Capabilities, Advantages, Key Features.

Phase-Locked Loops (PLLs): PLL Basics, PLL Ideal Behavior, PLL Errors.

Text Books:

3. Farzad Nekoogar and Faranak Nekoogar, ***From ASICs to SOCs: A Practical Approach***, Pearson Education, 2003, ISBN-10: 0-13-033857-5, ISBN-13: 978-0-13-033857-0

Recommended Reading:

5. Michael Smith, ***Application Specific Integrated Circuit***, Addison-Wesley, 1997, ISBN: 0201500221
6. Jari Nurmi, ***Processor Design: System-On-Chip Computing for ASICs and FPGAs***, Springer, 1st edition, 2007, ISBN: 1402055293
7. Douglas J. Smith, ***HDL Chip Design*** – a practical guide for designing, synthesizing and simulating ASICs and FPGAs using VHDL or Verilog, Doone Publications, 2000, ISBN: 0965193438

Low Power Digital VLSI Design (3 – 0 – 0)

MODULE – I **(11 hours)**

Introduction: Sources of power dissipation, Static power dissipation, Active power dissipation.

Circuit Techniques for Low-Power Design: Designing for low-power, Circuit techniques for leakage power reduction – Standby leakage control using transistor stacks, Multiple V_{th} techniques, Dynamic V_{th} technique, Supply voltage scaling technique, Leakage reduction techniques for chace(SRAM).

Low-Voltage Low-Power Adders: Standard adder cells – Half adders, Full adders and their various schematic configurations, CMOS addrer's architecture – Ripple carry adders, Carry look-ahead adders, Carry select adders, Carry save adders, Carry skip adders, Conditional sum adders, Performance valuation of various adder architectures, BiCMOS adders – PT-BiCMOS Gate, Low-voltage low-power design techniques – Trends of technology and power supply voltage, Low-voltage low-power logic styles, Current-mode adders – Current-mode CMOS adders using multiple-valued logic, Residue adders based on binary adders, Fast addition using single-digit number system.

MODULE – II **(12 hours)**

Low-Voltage Low Power Multipliers: Overview of multiplication – Unsigned multiplication, Shift/add multiplication algorithms, Multiplication of signed numbers, Types of multipliers architecture – Serial multipliers, Parallel multipliers, serial-parallel multipliers, Braun multiplier, Baugh-Wooley multiplier, Booth multiplier, Wallace tree multiplier.

Low-Voltage Low Power Read-Only Memories: Types of ROM, Basic physics of floating gate nonvolatile devices, Floating gate memories, Basics of ROM – Chip architecture, ROM cell arrays, Low-power ROM Technology – Sources of power dissipation, Low-power techniques at architecture level, Low-power techniques at circuit level.

Low-Voltage Low Power Static Random-Access Memories: Basics of SRAM, Memory cell, Pre-charge and equalization circuit, Decoder, Address transition detection, Sense amplifier, Output latch, Low-power SRAM technology – Sources of SRAM power, Development of low-power circuit techniques.

MODULE – III **(11 hours)**

Low-Voltage Low Power Static Random-Access Memories: Types of DRAM – Conventional DRAM, Fast page mode DRAM, Enhanced DRAM, Extended data out DRAM, Burst extended data output DRAM, Synchronous DRAM, Enhanced synchronous DRAM, Double data-rate DRAM, Synchronous link DRAM, Rambus DRAM, Direct rambus DRAM, Video RAM, Embedded DRAM, Basics of DRAM, Self-refresh Circuit, Half-voltage generator, Back-bias generator, Boosted-voltage generator, Reference-voltage generator, Voltage-down converter.

Large Low-Power VLSI System Design Applications: Behavioral level transform, Algorithm and architecture level transforms for low power – Differential coefficient for FIR filters, Algorithm using first-order differences, Algorithm using generalized *m*th-order differences, Negative differences, Sorted recursive differences, Shared multiplier based vector scaling operation, Architecture-driven voltage scaling, Power optimization using operation reduction, Power optimization using operation substitution, Precomputation based optimization for low power, Multiple and dynamic supply chain – Multiple supply voltage design, Dynamic supply voltage design, Choice of supply voltages, Rate of change of supply voltages, Power-supply network, Varying the clock speed, Varying the V_{DD} of RAM structure, Level conversion on the path from V_{DD}^{L} to V_{DD}^{H}.

Text Books:

1. Kiat-Seng Yeo and Kaushik Roy, ***Low-Voltage Low-Power VLSI Subsystems***, TMH Pvt. Ltd., 2009, ISBN-13: 978-0-07-067750-0, ISBN-10: 0-07-067750-6.
2. Kaushik Roy, Sharat C. Prasad, ***Low-Power CMOS VLSI Circuit Design*** , Wiley India Pvt Ltd, 2009, **ISBN:** 812652023X, **ISBN-13:** 9788126520237, 978-8126520237.

Recommended Reading:

4. Abdellatif Bellaouar and Mohamed Elmasry, ***Low-Power Digital VLSI Design: Circuits and Systems***, Kluwer Academic Publishers, 1995
5. Gary K. Yeap, ***Practical Low Power Digital VLSI Design***, Kluwer Academic Pub, 1998
6. Anantha P Chandrakasan, A P Chandrakasan and R W Brodersen, ***Low Power Digital CMOS Design***, Kluwer Academic Publishers, 1995, ISBN: 079239576X, EAN: 9780792395768.

Emerging Topics in IC Design (3 – 0 – 0)

MODULE – I **(11 hours)**

Review of MOS circuits: MOS and CMOS static plots, switches, comparison between CMOS and BI - CMOS.

MESFETS: MESFET and MODFET operations, quantitative description of MESFETS.

MIS structures and MOSFETS: MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS.

MODULE – II **(11 hours)**

Short channel effects and challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization

Beyond CMOS: Evolutionary advances beyond CMOS, carbon Nano tubes, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode- diode logic .Defect tolerant computing,

Super buffers, Bi-CMOS and Steering Logic: Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks - NMOS and CMOS functional blocks.

MODULE – III **(12 hours)**

Special circuit layouts and technology mapping: Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module lay out.

System design: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom Design.

Text Books:

1. Wayne Wolf, ***Modern VLSI Design***, Pearson Education, 2005 Third Edition.
2. Kevin F. Brennan, ***Introduction to Semiconductor Devices***, Cambridge University Press, 2005

Recommended Reading:

1. Eugene D Fabricius “Introduction to VLSI design”, McGraw-Hill International Publications, 1990
2. Michael Smith, ***Application Specific Integrated Circuit***, Addison-Wesley, 1997, ISBN: 0201500221

3. Douglas J. Smith, ***HDL Chip Design*** – a practical guide for designing, synthesizing and simulating ASICs and FPGAs using VHDL or Verilog, Doone Publications, 2000, ISBN: 0965193438

Introduction to Nanoelectronics (3 – 0 – 0)

MODULE – I **(11 hours)**

Introduction to Nanoelectronics: The "top-down" approach, The "bottom-up" approach, Nanoelectronis and nanotechnology potential.

Classical Particles, Classical Waves and Classical Quantum Particles: Comparison of classical and quantum systems, Origin of quantum mechanics, Light as a wave and light as a particle, Electrons as particles and electron as waves, Wavepackets and uncertainty.

Quantum Mechanics of Electrons: General postulates of quantum mechanics, Time-independent Schrodinger's equation, Analogies between quantum mechanics and classical electromagnetics, Probabilistic current density, Multiple particle systems, Spin and angular momentum.

Free and Confined Electrons: Free electrons, The free electron gas theory of metals, Electrons confined to a bounded region of space and quantum numbers, Fermi level and chemical potential, Partially confined electrons – Finite potential wells, Electrons confined to atoms – The hydrogen atom and the periodic table, Quantum dots wires and wells.

MODULE – II **(11 hours)**

Electrons Subject to a Periodic Potential – Band Theory of Solids: Crystalline materials, Electrons in a periodic potential, Kronig-Penney model of band structure, Band theory of solid – Doping in Semiconductors, Interacting systems model, The effect of an electric field on energy bands, Band structures of some semiconductors, Electronic bond transitions – interaction of electromagnetic energy and materials, Graphene and carbon nanotubes.

Tunnel Junctions and Applications of Tunneling: Tunneling through a potential barrier, Potential energy profiles for material interfaces, Applications of tunneling – Field emission, Gate-oxide tunneling and hot electron effects in MOSFETs, Scanning tunneling microscope, Double barrier tunneling and the resonant tunneling diode.

Coulomb Blockade and the Single-Electron Transistor: Coulomb blockade – Coulomb blockade in a nanocapacitor, Tunnel junctions, Tunnel junction excited by a current source, Coulomb blockade in a quantum dot circuit, The single electron transistor, Other SET and FET structures – Carbon nanotube transistor, Semiconductor nanowire FETs and SETs, Molecular SETs and molecular electronics.

MODULE – III **(12 hours)**

Particle Statistics and Density of States: Density of states in lower dimensions, Density of states in a semiconductor, Classical and quantum statistics – Carrier concentration in materials, The importance of the Fermi electrons, Equilibrium carrier concentration and the Fermi level in semiconductor.

Models of Semiconductor Quantum Wells, Quantum Wires and Quantum Dots: Semiconductor heterostructures and quantum wells, Quantum wires and nanowires, Quantum dots and nanoparticles, Fabrication techniques for nanostructures – Lithography, Nanoimprint lithography, Split-gate technology, Self-assembly.

Nanowires, Ballistic Transport and Spin Transport: Classical and semiclassical transport – Classical theory of conduction – free electron gas model, Semiclassical theory of electrical conduction – Fermi gas model, Classical resistance and conductance, Conductivity of metallic nanowires – the influence of wire radius, Ballistic transport – Electron collisions and length scales, Ballistic transport model, Quantum resistance and conductance, Origin of quantum resistance, Carbon nanotubes and nanowires, Transport of spin and spintronics – the transport of spin, Sprintonic devices and applications.

Text Books:

1. George W. Hanson, ***Fundamentals of Nanoelectronics***, Pearson Education, 2009, ISBN: 978-81-317-2679-2.

Recommended Reading:

1. Vladimir V. Mitin, Viatcheslav A. Kochelap and Michael A. Stroscio, ***Introduction to Nanoelectronics*** Science, Nanotechnology, Engineering, and Applications, Cambridge University Press, 2008, ISBN: 978-0-521-88172-2
2. M. Kuno, ***Introduction to Nanoscience and Nanotechnology: A Workbook***, http://nd.edu/~mkuno/Class_downloads/Chem647_nano_text.pdf
3. G.L. Hornyak, H.F. Tibbals, Joydeep Dutta, and J.J. Moore,***Introduction to Nanoscience & Nanotechnology***, CRC Press, 2008 **ISBN:** 9781420047790 **ISBN 10:** 1420047795.
4. Jeremy Ramsden, ***Essentials of Nanotechnology***, BOOKBOON.com, ISBN 978-87-7681-418-2

Statistical Signal Processing (3 – 0 – 0)

Module – 1 **(9 hrs)**

Discrete Random Process: Random Process- Ensemble Average, Gaussian Process, Stationary Process, The Autocorrelation and Autocovariance Matrix, Ergodicity, White Noise, The Power Spectrom, Filtering Random Process, Special Types of Random Process-ARMV Process, AR Process, MA Process, Harmonic Process. [Read Hayes Chapter 3.3.1 – 3.3.8, 3.4, 3.6.1 – 3.6.4]

Signal Modeling: Introduction, Stochastic Models- ARMA Models, AR Models, MA Models, Application: Power Spectrum Estimation. [Read Hayes Chapter 4.1, 4.7.1 – 4.7.4]

Module – 2 **(18 hrs)**

Winer Filtering: Introduction, The FIR Wiener Filter- Filtering, Linear Prediction, Noise Cancellation, IIR Wiener Filter- Noncausal IIR Wiener Filter, The Causal IIR Wiener Filter, Causal Wiener Filtering, Causal Linear Prediction, Wiener Deconvolution, Discrete Kalman Filter. [Read Hayes Chapter 7.1, 7.2.1 – 7.2.3, 7.3.1 – 7.3.5, 7.4)

Spectrum Estimation: Introduction, Nonparametric Method- The Periodogram, Performance of Periodogram. Parametric Methods- AR Spectrum Estimation, MA Spectrum Estimation, ARMA Spectrum Estimation. Frequency Estimation- Eigendecomposition of the Autocorrelation Matrix, MUSIC. [Read Hayes Chapter 8.1, 8.2.1, 8.2.2, 8.5.1 – 8.5.3, 8.6.1, 8.6.3]

Module – 3 **(11 hrs)**

Adaptive Filtering: Introduction, FIR Adaptive Filters- The Steepest Descent Adaptive Filter, The LMS Algorithm, Convergence of LMS Algorithm, NLMS, Noise Cancellation, LMS Based Adaptive Filter, Channel Equalization, Adaptive Recursive Filter, RLS- Exponentially Weighted RLS, Sliding Window RLS. [Read Hayes Chapter 9.1, 9.2.1 – 9.2.6, 9.2.9, 9.3, 9.4]

Text Book

1. Monson H. Hayes, Statistical Digital Signal Processing & Modeling, John Wiley & Sons

Reference Books

1. Steven M. Kay, Fundamentals of Statistical Signal Processing: Estimation Theory, Prentice Hall.

Adaptive Signal Processing (3 – 0 – 0)

MODULE – I **(11 hours)**

Adaptive System: Definition and Characteristics, Areas of Application, Example of an Adaptive System, Adaptive Linear Combiner, The Performance Function, Gradient and Minimum Mean-Square Error, Alternative Expression of the Gradient, Decorrelation of Error and Input Components. [Read Widrow: Chapter 1 and 2]

Winer Filter: Linear Optimum Filtering, Principle of Orthogonality, Minimum Mean Square Error, Winer-Hopf Equation, Error Performance Surface. [Read Haykin: Chapter 2.1-2.5]

Linear Prediction: Forward Linear Prediction, Backward Linear Prediction, Properties of Prediction Error Filters. [Read Haykin: Chapter 3.1, 3.2, 3.4]

MODULE – II **(11 hours)**

Method of Steepest Descent: Basic Idea of Steepest-Descent Algorithm, Steepest-Descent Algorithm Applied to Winer Filter, Stability of Steepest-Descent Algorithm, Limitations of Steepest-Descent Algorithm. [Read Haykin: Chapter 4.1 – 4.3, 4.6]

Least-Mean Square Adaptive Filter: Overview, LMS Adaptation Algorithm, Application, Comparison of LMS With Steepest-Descent Algorithm. [Read Haykin: Chapter 5.1 – 5.3, 5.5]

Normalized Least-Mean Square Adaptive Filter: Normalized LMS Filter as the Solution to Constrained Optimization Problem, Stability of the NLMS. [Read Haykin: Chapter 6.1, 6.2]

MODULE – III **(11 hours)**

Frequency-Domain and Subband Adaptive Filters: Block Adaptive Filters [Read Haykin: Chapter 7.1]

RLS Adaptive Filters: Statement of Linear Least-Square Estimation Problem, Matrix Inversion Lemma, The Exponentially Weighted RLS Algorithm. [Read Haykin: Chapter 8.1, **9.1 – 9.3]**

Kalman Filter: Recursive Minimum Mean-Square Estimation For Scalar Random Variable, Kalman Filtering Problem, Initial Conditions, Summary of Kalman Filter. [Read Haykin: Chapter 10.1, 10.2, 10.6, 10.7]

Text Books

1. Bernard Widrow and Samuel D. Stearns, Adaptive Signal Processing, Pearson Education

2. Simon Haykin, Adaptive Filter Theory (Fourth Edition), Pearson Education

Reference Books

1.