BIJU PATNAIK UNIVERSITY OF TECHNOLOGY, ORISSA

Syllabus for M.Tech in VLSI & Embedded System Design

Semester	Subject	Credit	Details of Subjects
I	PC-1	4	HDL and High Level Synthesis
	PC-2	4	Digital Integrated Circuit Design
	PC-3	4	Semiconductor Device Modeling and Simulation
	EL-1	3	VLSI Fabrication Technology
	(***any one***)		VLSI Digital Signal Processing Systems
			VLSI Testing
	EL-2	3	Analogue Integrated Circuit Design
	(***any one***)		VLSI Physical Design
			Reliability and Testability of IC Design
	Lab-1	4	EDA Lab
	Seminar-1	2	Seminar on Pre-thesis work-1
Semester Credits:		**24**	
II	PC-4	4	Embedded System Design
	PC-5	4	RF and Mixed-Signal Integrated Circuits
	EL-3	3	Microsystems – Principles, Design and Application
	(***any one***)		Analogue and Mixed-Signal Testing
			VLSI and MEMS Packaging
	EL-4	3	ASIC and SoC Design
	(***any one***)		Low Power Digital VLSI Design
			Emerging Topics in IC Design
	EL-5	3	Nanotechnology
	(***any one***)		Statistical Signal Processing
			Adaptive Signal Processing
	Lab-2	4	Embedded System Lab
	Seminar-2	2	Seminar on Pre-thesis work-2
	Viva-1	2	Comprehensive Viva-Voce - I
Semester Credits:		**25**	

Semester	Subject	Credit	Details of Subjects
III	**Open Elective** **(any one)** **Thesis-1**	**3** **14**	Project Management / Project Costing / Technology Management / Research Methodology / Optimization Techniques / Computational Intelligence / Thesis – I
Semester Credits:		**17**	
IV	Thesis -2 Seminar-2 Viva-2	20 2 2	Thesis – II Seminar Comprehensive Viva-Voce – II
Semester Credits:		**24**	
Total Credits		**90**	

HDL and High Level Synthesis (3 – 1 – 0) Credits: 4

MODULE – I **(13 hours)**

Structured Design Concepts:

The Abstraction Hierarchy, Textual vs. Pictorial Representations, Types of Behavioral Descriptions, Design Process, Structural Design Decomposition, The Digital Design Space

Design Tools:

CAD Tool Taxonomy, Schematic Editors, Simulators, The Simulation System, Simulation Aids, Applications of Simulation, Synthesis Tools

Basic Features of VHDL:

Major Language Constructs, Lexical Description, VHDL Source File, Data Types, Data Objects, Language Statements, Advanced Features of VHDL, The Formal Nature of VHDL, VHDL 93

Basic VHDL Modeling Techniques:

Modeling Delay in VHDL, The VHDL Scheduling Algorithm, Modeling Combinational and Sequential Logic, Logic Primitives

MODULE – II **(13 hours)**

Algorithmic Level Design:

General Algorithmic Model Development in the Behavioral Domain, Representation of System Interconnections, Algorithmic Modeling of Systems

Register Level Design:

Transition from Algorithmic to Data Flow Descriptions, Timing Analysis, Control Unit Design, Ultimate RISC Machine

Gate Level; and ASIC Library Modeling:

Accurate Gate Level Modeling, Error Checking, Multivalued Logic for Gate Level Modeling, Configuration Declarations for Gate Level Models, Modeling Races and Hazards, Approaches to Delay Control

HDL-Based Design Techniques:

Design of Combinational Logic Circuits, Design of Sequential Logic Circuits

MODULE – III **(14 hours)**

ASICs and the ASIC Design Process:

What is an ASIC?, ASIC Circuit Technology, Types of ASICs, The ASIC Design Process, FPGA Synthesis

Modeling for Synthesis:

Behavioral Model Development, The Semantics of Simulation and Synthesis, Modeling Sequential Behavior, Modeling Combinational Circuits for Synthesis, Inferred Latches and Don't Cares, Tristate Circuits, Shared Resources, Flattening and Structuring, Effect of Modeling Style on Circuit Complexity

Integration of VHDL into a Top-Down Design Methodology:

Top-Down Design Methodology, Sobel Edge Detection Algorithm, System Requirements Level, System Definition Level, Architecture Design, Detailed Design at the RTL Level, Detailed Design at the Gate Level

Synthesis Algorithms for Design Automation:

Benefits of Algorithmic Synthesis, Algorithmic Synthesis Tasks, Scheduling Techniques, Allocation Techniques, State of the Art in High-Level Synthesis, Automated Synthesis of VHDL Constructs

Textbooks:

1. James R. Armstrong and F. Gail Gray, ***VHDL Design Representation and Synthesis***, Prentice Hall, 2000.

Recommended Reading:

1. A.M. Dewey, ***Analysis and Design of Digital Systems with VHDL***, PWS Kent, 1996.
2. A.A. Jerraya, H. Ding and P. Kission, ***Behavioral Synthesis and Component Reuse with VHDL***, Kluwer, 1996.
3. K.C. Chang, ***Digital System Design with VHDL and Synthesis: An Integrated Approach***, Wiley India Pvt. Ltd., New Delhi

Digital Integrated Circuit Design (3 – 1 – 0) Credits: 4

MODULE – I (13 hours)

Introduction, Design Metrics and Manufacturing Process:
A Historical Perspective, Issues in Digital Integrated Circuit Design, Quality Metrics of a Digital Design, Introduction to Manufacturing Process, Manufacturing CMOS Integrated Circuits, Design Rules – The Contract between Designer and Process Engineer, Packaging Integrated Circuits

The Devices:
Introduction, The Diode, The MOS(FET) Transistor, The Wire, Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, SPICE Wire Models

The CMOS Inverters and CMOS Logic Gates – the Static View:
Introduction to CMOS Inverter, The Static CMOS Inverter – An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter, Introduction to Static CMOS Design, Complementary CMOS, Ratioed Logic, Pass-Transistor Logic

CMOS Inverter – the Dynamic View:
Performance of CMOS Inverter: The Dynamic Behavior, Power, Energy, and Energy-Delay, Perspective: Technology Scaling and its Impact on the Inverter Metrics

MODULE – II (13 hours)

Dynamic CMOS Logic, Timing Metrics:
Dynamic CMOS Design, CMOS Logic Design Perspectives, Timing Metrics: Timing Metrics for Sequential Circuits, Classification of Memory Elements

Static and Dynamic Sequential Circuits:
Static Latches and Registers, Dynamic Latches and Registers, Alternative Register Styles: Pulse Registers and Sense-Amplifier Based Registers, Pipelining: An Approach to Optimize Sequential Circuits – Latch Vs Register-Based Pipelines and NORA-CMOS – A Logic Style for Pipelined Structures, Nonbistable Sequential Circuits

Coping with Interconnect:
Introduction, Capacitive Parasitics, Resistive Parasitics, Inductive Parasitics, Advanced Interconnect Techniques, Networks-on-a-Chip

Timing Issues in Digital Circuits:
Introduction, Timing Classification of Digital Systems, Synchronous Design – An In-depth Perspective, Self-Timed Circuit Design, Synchronisers and Arbiters, Clock Synthesis and Synchronisation Using a Phase-Locked Loop, Future Directions and Perspectives

MODULE – III (14 hours)

Designing Arithmetic Building Blocks:
Introduction, Datapaths in Digital Processor Architecture, The Adder, The Multiplier, The Shifter, Other Arithmetic Operators, Power and Speed Trade-off's in Datapath Structures, Perspective: Design as a Trade-off

Designing Memory and Array Structures:
Introduction, The Memory Core, Memory Peripheral Circuitry, Memory Reliability and Yield, Power Dissipation in Memories, Case Studies in Memory Design: The PLA, A 4-Mbit SRAM and A 1-Gbit NAND Flash memory, Perspective: Semiconductor Memory Trends and Evolution

Validation and Test of Manufactured Circuits:
Introduction, Test Procedure, Design for Testability, Test Pattern Generation

Textbooks:

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, ***Digital Integrated Circuits – A Design Perspective*****,** 2nd edn., Pearson Education, 2003. ISBN: 8178089912.

Recommended Reading:

1. K. Eshraghian, and N.H.E. Weste, ***Principles of CMOS VLSI Design – a Systems Perspective***, 2nd edn., Addison Wesley, 1993.
2. Wayne Wolf, ***Modern VLSI Design System – on – Chip Design***, 3rd edn., Pearson Education, 2003.
3. M. Michael Vai, ***VLSI Design***, CRC Press, 2001.
4. John P. Uyemura, ***CMOS Logic Circuit Design***, Springer (Kluwer Academic Publishers), 2001.
5. Ken Martin, ***Digital Integrated Circuit Design***, Oxford University Press, 2000.

Semiconductor Device Modeling and Simulation (3–1–0) Credits: 4

MODULE – I **(13 hours)**

Semiconductor Electronics Review:
Elements of Semiconductor Physics, Physical Operation of a ***PN*** Junction, MOS Junction, MS Junction

PN–Junction Diode and Schottky Diode:
DC Current-Voltage Characteristics, Static Model, Large-Signal Model, Small-Signal Model, Schottky Diode and its Implementation in SPICE2, Temperature and Area Effects on the Diode Model Parameters, SPICE3, HSPICE and PSPICE Models

Bipolar Junction Transistor (BJT):
Transistor Convention and Symbols, Ebers-Moll Static Model, Ebers-Moll Large-Signal Model, Ebers-Moll Small-Signal Model, Gummel-Poon Static Model, Gummel-Poon Large-Signal Model, Gummel-Poon Small-Signal Model, Temperature and Area Effects on the BJT Model Parameters, Power BJT Model, SPICE3, HSPICE and PSPICE Models

MODULE – II **(13 hours)**

Junction Field-Effect Transistor (JFET):
Static Model, Large-Signal Model and its Implementation in SPICE2, Small-Signal Model and its Implementation in SPICE2, Temperature and Area Effects on the JFET Model Parameters, SPICE3, HSPICE and PSPICE Models

Metal-Oxide-Semiconductor Transistor (MOST):
Structure and Operating Regions of the MOST, LEVEL1 Static Model, LEVEL2 Static Model, LEVEL1 and LEVEL2 Large-Signal Model, LEVEL3 Static Model, LEVEL3 Large-Signal Model, The Effect of Series Resistances, Small-Signal Models, The Effect of Temperature, BSIM1, BSIM2, SPICE3, HSPICE and PSPICE Models

MODULE – III **(14 hours)**

BJT Parameter Measurements:
Input and Model Parameters, Parameter Measurements

MOST Parameter Measurements:
LEVEL1 Model Parameters, LEVEL2 Model (Long-Channel) Parameters, LEVEL2 Model (Short-Channel) Parameters, LEVEL3 Model Parameters, Measurements of Capacitance, BSIM Model Parameter Extraction

Noise and Distortions:

Noise, Distortion

Metal-Semiconductor Field-Effect Transistor (MESFET), Ion-Sensitive Field-Effect Transistor (ISFET) and Semiconductor-Controlled Rectifier (Thyristor):

The MESFET, The ISFET, The Thyristor

Textbooks:

1. Paolo Antognetti and Giuseppe Massobrio, ***Semiconductor Device Modeling with SPICE,*** 2nd edn., McGraw-Hill, New York, 1993, ISBN 0071349553 (paperback) or 007 0024693 (hardback).

Recommended Reading:

1. Richard S. Muller, Theodore I. Kamins, and Mansun Chan, ***Device Electronics for Integrated Circuits***, 3rd edn., John Wiley and Sons, New York, 2003. ISBN: 0-471-59398-2. Listed as D
2. H. Craig Casey, ***Devices for Integrated Circuits: Silicon and III-V Compound Semiconductors***, John Wiley, New York, 1999. Listed as DI
3. Dieter K. Schroder, ***Semiconductor Material and Device Characterization***, John Wiley and Sons, New York, 1990. Listed as S

VLSI Fabrication Technology

(3 – 0 – 0) Credits: 3

MODULE – I **(11 hours)**

Introduction:

Moore's Law and material processing, Defects in crystals, Eutectic phase diagram, Solid solubility, Homogeneous nucleation, Heterogeneous Nucleation, Growth processes

Crystal Growth:

Necking and dislocation free CZ crystal growth, Segregation of impurities along length and diameter, Defects in CZ crystals, FZ Crystal growth

Epitaxy:

Vapour phase epitaxy, LPE, MBE, CVD deposition of Polysilicon, SILOX Process

Diffusion:

Constant & limited source diffusion, Concentration dependent diffusion, Field assisted diffusion, Junction depth, Open tube and closed tube diffusion, Diffusion sources.

MODULE – II **(11 hours)**

Ion Implantation:

Basic process, Ion Implantation Systems, Ion penetration and profile, Ion Implantation Damage, Annealing

Oxidation:

Purpose, Dry and wet oxidation, Deal-Grove model, Oxidation system, Properties of oxides – Masking and charges in oxides

Deposition Processes:

Fundamentals of vacuum systems, Vacuum evaporation of thin films, DC and RF Sputtering of thin films, Interconnects, Contacts and dielectrics in IC Fabrication, Deposition of Silicon Nitride, Silicides and insulating layers

Lithography:

Pattern generation and mask making, Optical Lithography – Contact, Proximity and Projection Printing, Photoresists – Negative, Positive, Lift-off process, Electron beam and X-ray lithographic techniques.

MODULE – III **(12 hours)**

Etching:

Wet Etching, Isotropic and Anisotropic Etching, Plasma Etching, Reactive Ion Beam Etching.

IC Process Integration:

Bipolar Transistor Fabrication, Isolation techniques, P-MOS, N-MOS and C-MOS processes, IC Fabrication Process Integration, IC Process Yield and Reliability

MEMS Fabrication Processes:

Micro machining, Bulk Micro machining, Surface Micro machining, Deep RIE, Advanced Lithography, HEXIL & SCREAM Process, Polymer molding and LIGA Process

Text Books:

1. S.K. Gandhi, ***VLSI Fabrication Principles: Silicon and Gallium Arsenide***, Wiley India Pvt. Ltd., New Delhi, 2nd edn. (1994), ISBN: 0471580058.
2. Marc J. Madou, ***Fundamentals of Microfabrication***, CRC Press (2002), ISBN: 0849308267

Reference Books:

1. J. Plummer, M. Deal and P. Griffin, ***Silicon VLSI Technology***, Prentice Hall, 2000, ISBN: 0130850373.
2. S.M.Sze, ***VLSI Technology***, Tata McGraw Hill, 1983, ISBN: 0070582912.
3. S.Mahajan, ***Principles of Growth and Processing of Semiconductors***, McGraw Hill International Book Company, 1999, ISBN: 0070396051.
4. S.A.Campbell, ***The Science and Engineering of Microelectronics Fabrication***, Oxford University Press, ISBN: 0195105087.

VLSI Digital Signal Processing Systems (3 – 0 – 0) Credits: 3

MODULE – I (11 hours)

Introduction to DSP System:

Typical DSP algorithms, DSP application demands and scaled CMOS technology, Representation of DSP algorithms.

Iteration Bound:

Data-flow graph representations, Loop bound and iterartion bound, Algorithms for computing iteration bound, Iteration bound of multirate data-flow graphs.

Pipelining and Parallel Processing:

Pipelining of FIR digital filters, Parallel processing, Pipelining and parallel processing for low power.

Retiming:

Definitions and properties, Solving systems of inequalities, Retiming techniques.

MODULE – II (11 hours)

Unfolding:

An algorithm for unfolding, Properties of unfolding, Critical path, unfolding and retiming, Applications of unfolding.

Folding:

Folding transformation, Register minimization techniques, Register minimization in folding architectures, Folding of multirate systems.

Systolic Architecture Design:

Systolic array design methodology, FIR systolic arrays, Selection of scheduling vector, Matrix-matrix multiplication and 2D systolic array design, Systolic design for space representations containing delays.

MODULE – III (12 hours)

Bit-Level Arithmetic Architecture:

Parallel multipliers, Interleaved floor-plan and bit-plane-based digital filters, Bit-serial multipliers, Bit-serial filter design and implementation, Canonic signed digit arithmetic, Distributed arithmetic.

Programmable Digital Signal Processors:

Evolution of programmable digital signal processors, Important features of DSP processors, DSP processors for mobile and wireless communications, Processors for multimedia signal processing.

Textbooks:

1. K. K. Parhi, ***VLSI Digital Signal Processing Systems*, *Design and Implementation***, Wiley India Pvt. Ltd., New Delhi, ISBN 10: – 8126510986, ISBN – 13: 9788126510986.

Recommended Reading:

1. K.P. Keshab, ***VLSI Digital Signal Processing Systems: Design and Implementation***, Jacaranda Wiley, 1999.
2. Richard J, Higgins, ***Digital Signal Processing in VLSI***, Prentice Hall, ISBN-10: 013212887X, ISBN-13: 9780132128872
3. M.A. Bayoumi, ***VLSI Design Methodology for DSP Architectures***, Kluwer, 1994.

VLSI Testing

(3 – 0 – 0) Credits: 3

MODULE – I **(11 hours)**

VLSI Physical Design Automation:

VLSI Design Cycle, Physical Design Cycle, Design Styles, System Packaging Styles, Historical Perspectives, Existing Design Tools

MODULE – II **(11 hours)**

Data Structure and Basic Algorithms:

Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithm for Physical Design

MODULE – III **(12 hours)**

Placement:

Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement

Text Books:

1. Michael L. Bushnell and Vishwani D. Agrawal, ***Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits***, B.S.Publications**,** 2000, ISBN 10: **–** 0792379918, ISBN-13: – 9780792379911.

Reference Books:

1. L.-T. Wang, C.-W. Wu, and X. Wen, ***VLSI Test Principles and Architectures: Design for Testability (Systems on Silicon)***, Morgan Kaufmann, ISBN 10: **–** 0123705975.
2. Alfred L. Crouch, ***Design-for-Test for Digital IC's and Embedded Core Systems***, Prentice Hall, ISBN 10: **–** 0130848271.
3. Niraj Jha and Sandeep Gupta, ***Testing of Digital Systems***, Cambridge University Press, 2003, ISBN 10: **–** 0521773563.

Analogue Integrated Circuit Design (3 – 0 – 0) Credits: 3

MODULE – I (11 hours)

Introduction:

The MOS Transistor, I-V Characteristics, Equivalent Circuits, Noise

Resistor, Capacitors and Switches:

Integrated Resistors, Integrated Capacitors, Analog Switches, Layout of Switches

Basic Building Blocks:

Inverter with Active Load, Cascode, Cascode with Cascode Load, Source Follower, Threshold Independent Level Shift, Improved Output Stages

MODULE – II (11 hours)

Current and Voltage Sources:

Current Mirrors, Current References, Voltage Biasing, Voltage References

CMOS Operational Amplifiers:

General Issues, Performance Characteristics, Basic Architecture, Two Stages Amplifier, Frequency Response and Compensation, Slew Rate

MODULE – III (12 hours)

Operational Amplifiers and OTAs

Design of Two Stage OTAs: Guidelines, Single Stage Schemes, Class AB Amplifiers, Fully Differential Op-Amps, Micro-Power OTAs, Noise Analysis, Layout

CMOS Comparators:

Performance Characteristics, General Design Issues, Offset Compensation, Latches

Textbooks:

3. Franco Maloberti, ***Analog Design for CMOS VLSI Systems***, Kluwer Academic Publishers, 2001. ISBN: 0-7923-7550-5.

Reference Books:

1. Behzad Razavi, ***Design of Analog CMOS Integrated Circuits***, McGraw-Hill, 2001. ISBN: 0-07-238032-2.
2. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, ***Analysis and Design of Analog Integrated Circuit***, John Wiley & Sons, Inc., 4th edn., 2000. ISBN: 0-471-32168-0.
3. Phillip E. Allen and Douglas R. Holberg, ***CMOS Analog Circuit Design***, Oxford University Press, 2nd edn., 2002. ISBN: 0-19-511644-5
4. Johan H. Huijsing, ***Operational Amplifiers – Theory and Design,*** Kluwer. ISBN: 0792372840

VLSI Physical Design

(3 – 0 – 0) Credits: 3

MODULE – I **(11 hours)**

VLSI Physical Design Automation:

VLSI Design Cycle, Physical Design Cycle, Design Styles, System Packaging Styles, Historical Perspectives, Existing Design Tools

Design and Fabrication of VLSI Devices:

Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules, Layout of Basic Devices

Fabrication Process and its Impact on Physical Design:

Scaling Methods, Status of Fabrication Process, Issues Related to the Fabrication Process, Future of Fabrication Process, Solutions for Interconnect Issues, Tools for Process Development

MODULE – II **(11 hours)**

Data Structure and Basic Algorithms:

Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithm for Physical Design

Partitioning:

Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithm, Simulated Annealing and Evolution, Other Partitioning Algorithms, Performance Driven Partitioning

Floor Planning and Pin assignment:

Floor Planning, Chip Planning, Pin Assignment, Integrated Approach

MODULE – III **(12 hours)**

Placement:

Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement

Over-the-Cell Routing and Via Minimisation, Clock and Power Routing:

Over-the-Cell Routing, Via Minimisation, Clock Routing, Power and Ground Routing

Physical Design Automation of FPGAs:

FPGA Technologies, Physical Design Cycle for FPGAs, Partitioning, Routing

Physical Design Automation of MCMs:

MCM Technologies, MCM Physical Design Cycle, Partitioning, Placement, Routing

Text Books:

1. Naved A. Sherwani, ***Algorithms for VLSI Physical Design Automation***, 3rd Edn., Springer (India) Pvt. Ltd., 2005, ISBN: 0792383931

Reference Books:

1. Gerez, ***Algorithms for VLSI Design Automation***, Wiley India Pvt. Ltd., New Delhi, ISBN 10: – 8126508211, ISBN 13: – 9788126508211.

Reliability and Testability of IC Design (3 – 0 – 0) Credits: 3

MODULE – I (11 hours)

Basic Concepts, Quality and Reliability Assurance of Complex Equipments and Systems:
Introduction, Basic Concepts, Basic Tasks and Rules for Quality and Reliability Assurance of Complex Equipments and Systems

Probability Theory, Stochastic Process and Mathematical Statistics for Reliability Analysis:
Concept of Probability, Random Variables and Random Vectors, Distribution Functions used in Reliability Analysis, Limit Theorems, Renewal Processes, Regenerative and Semi-Regenerative Processes, Markov and Semi-Markov Processes, Non-regenerative Stochastic processes, Empirical Methods in Mathematical Statistics, Parameter Estimation, Testing Statistical Hypotheses

Reliability Analysis During the Design and Development Phases:
Introduction, Predicted Reliability of Equipments and Systems with Simple Structure, Reliability of Systems with Complex Structure, Reliability Allocation, Mechanical Reliability, Drift Failure, Failure Mode Analyses, Reliability Aspects in Design Reviews

MODULE – II (11 hours)

Qualification Tests for Components and Assemblies:
Basic Selection Criteria for Electronic Components, Qualification Tests for Complex Electronic Components, Failure Modes, Failure Mechanisms, and Failure Analysis of Electronic Components, Qualification Tests for Electronic Assemblies

Maintainability Analysis:
Maintenance and Maintainability, Maintenance Concepts, Maintainability Aspects in Design reviews, Predicted Maintainability, Basic Models for Spare Part Provisioning, Cost Considerations

Design Guidelines for Reliability, Maintainability and Software Quality:
Design Guidelines for Reliability, Design Guidelines for Maintainability, Design Guidelines for Software Quality

MODULE – III (12 hours)

Reliability and Availability of Repairable Systems – II:
Introduction and General Assumptions, One-Item Structure, Systems with Redundancy, 1-out-of-2 Redundancy, ***k***-out-of-***n*** Redundancy, Simple Series-Parallel Structures, Approximate Expressions for Large Series-Parallel Structures, Systems with Complex Structures, Computer-Aided Reliability and Availability Computations

Statistical Quality Control and Reliability Tests:
Statistical Quality Control, Statistical Reliability Tests, Statistical Maintainability Tests, Accelerated Testing, Goodness-of-fit Tests, Statistical Analysis of General Reliability Data

Quality and Reliability Assurance During the Production Phase:
Basic Activities, Testing and Screening of Electronic Components, Test and Screening Strategies, Economic Aspects, Reliability Growth

Text Books:

1. Alessandro Birolini, ***Reliability Engineering Theory and Practice***, 4th Edn., Springer (India) Pvt. Ltd., 2006, ISBN: 8181284518

Reference Books:

1. P.K. Lala, ***Digital Circuit Testing and Testability***, Academic Press, 1997
2. M.T.C. Lee, ***High-Level Test Synthesis of Digital VLSI Circuits***, Artech, 1997
3. P. Mazumdar and K. Chakreborty, ***Testing & Testable Design of High Density Random Access Memories***, Kluwer, 1996